IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Atty Dkt. 829-618
C# M#

YONEMARU, M. TC/A.U. 2826

Serial No. 10/720,764 Examiner: Dickey, T.

Filed: November 25, 2003 Date: April 27, 2006

Title: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS CONNECTED IN SERIES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE/AMENDMENT/LETTER

This is a response/amendment/letter in the above-identified application and includes an attachment which is hereby incorporated by reference and the signature below serves as the signature to the attachment in the absence of any other signature thereon.

☐ **Correspondence Address Indication Form Attached.**

Fees are attached as calculated below:

Total effective claims after amendment **22** minus highest number previously paid for **23** (at least 20) = 0 x $50.00	$0.00 (1202)/$0.00 (2202)	$
Independent claims after amendment **2** minus highest number previously paid for **3** (at least 3) = 0 x $200.00	$0.00 (1201)/$0.00 (2201)	$
If proper multiple dependent claims now added for first time, (ignore improper); add	$360.00 (1203)/$180.00 (2203)	$
Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s) — One Month Extension $120.00 (1251)/$60.00 (2251); Two Month Extensions $450.00 (1252)/$225.00 (2252); Three Month Extensions $1020.00 (1253/$510.00 (2253); Four Month Extensions $1590.00 (1254/$795.00 (2254); Five Month Extensions $2160.00 (1255/$1080.00 (2255)		$
Terminal disclaimer enclosed, add	$130.00 (1814)/ $65.00 (2814)	$
☐ Applicant claims "small entity" status. ☐ Statement filed herewith		
Rule 56 Information Disclosure Statement Filing Fee	$180.00 (1806)	$
Assignment Recording Fee	$40.00 (8021)	$
Other:		$
	TOTAL FEE ENCLOSED	$ **0.00**

The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

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NIXON & VANDERHYE P.C.
By Atty: Joseph A. Rhoa, Reg. No. 37,515

Signature: _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

YONEMARU, M. Atty. Ref.: 829-618; Confirmation No. 3114

Appl. No. 10/720,764 TC/A.U. 2826

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For: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS CONNECTED IN SERIES

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April 27, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION

Responsive to the Official Action dated January 27, 2006, reconsideration is respectfully requested for at least the following reasons.